I. IN THE CLAIMS

Please cancel claims 1-40 and 45-84 without prejudice.

41. (Original) An electrically programmable and erasable memory device comprising:

a substrate of semiconductor material of a first conductivity type;

first and second spaced-apart terminals in the substrate of a second conductivity type, with a channel region therebetween;

a first insulation layer disposed over said substrate;

an electrically conductive floating gate disposed over said first insulation layer and extending over a portion of said channel region and over a portion of the second terminal;

a second insulation layer disposed over and adjacent the floating gate and having a thickness permitting Fowler-Nordheim tunneling of charges therethrough; and

an electrically conductive control gate having a first portion and a second portion, the first portion being substantially rectangularly shaped and positioned immediately adjacent to the second insulation layer, the second portion being substantially a spacer connected to the first portion and disposed over the floating gate and insulated therefrom.

42. (Original) The device of claim 41, wherein the control gate forms a notch at the connection between the first portion and the second portion.

43. (Original) An array of electrically programmable and erasable memory devices comprising:

a substrate of semiconductor material of a first conductivity type;

spaced apart isolation regions formed on the substrate which are substantially parallel to one another and extend in a first direction, with an active region between each pair of adjacent isolation regions;

each of the active regions including a column of memory cells extending in the first direction, each of the memory cells including:

first and second spaced-apart terminals formed in the substrate having a second conductivity type, with a channel region formed in the substrate therebetween,

a first insulation layer disposed over said substrate including over said channel region,

an electrically conductive floating gate disposed over said first insulation layer and extending over a portion of said channel region and over a portion of the second terminal, and

a second insulation layer disposed over and adjacent the floating gate and having a thickness permitting Fowler-Nordheim tunneling of charges therethrough; and

a plurality of electrically conductive control gates each extending across the active regions and isolation regions in a second direction substantially perpendicular to the first direction and having a first portion that is substantially rectangular in shape and a second portion that is connected to the first portion and is substantially a spacer, wherein each of the control gates intercepts one of the memory cells in each of the active regions such that the first portion is positioned immediately adjacent to the second insulation layer therein and the second portion is disposed over the floating gate and insulated therefrom.

44. (Original) The device of claim 43, wherein the control gate forms a notch at the connection between the first portion and the second portion.

85. (Original) An electrically programmable and erasable memory device comprising:

a substrate of semiconductor material of a first conductivity type;

first and second spaced-apart terminals in the substrate of a second conductivity type, with a channel region therebetween;

a first insulation layer disposed over said substrate;

an electrically conductive floating gate disposed over said first insulation layer and extending over a portion of said channel region and over a portion of the second terminal;

a second insulation layer disposed over and adjacent the floating gate and having a thickness permitting Fowler-Nordheim tunneling of charges therethrough; and

an electrically conductive control gate having a first portion and a second portion, the first portion having a substantially planar sidewall portion and is positioned immediately adjacent to the second insulation layer, the second portion being substantially a spacer connected to the substantially planar sidewall portion and disposed over the floating gate and insulated therefrom.

86. (Original) The device of claim 85, wherein the control gate forms a notch at the connection between the first portion and the second portion.

87. (Original) An array of electrically programmable and erasable memory devices comprising:

a substrate of semiconductor material of a first conductivity type;

spaced apart isolation regions formed on the substrate which are substantially parallel to one another and extend in a first direction, with an active region between each pair of adjacent isolation regions;

each of the active regions including a column of memory cells extending in the first direction, each of the memory cells including:

first and second spaced-apart terminals formed in the substrate having a second conductivity type, with a channel region formed in the substrate therebetween,

a first insulation layer disposed over said substrate including over said channel region,

an electrically conductive floating gate disposed over said first insulation layer and extending over a portion of said channel region and over a portion of the second terminal, and

a second insulation layer disposed over and adjacent the floating gate and having a thickness permitting Fowler-Nordheim tunneling of charges therethrough; and

a plurality of electrically conductive control gates each extending across the active regions and isolation regions in a second direction substantially perpendicular to the first direction and having a first portion that has a substantially planar sidewall portion and a second

portion that is connected to the substantially planar sidewall portion and is substantially a spacer, wherein each of the control gates intercepts one of the memory cells in each of the active regions such that the first portion is positioned immediately adjacent to the second insulation layer therein and the second portion is disposed over the floating gate and insulated therefrom.

88. (Original) The device of claim 87, wherein the control gate forms a notch at the connection between the first portion and the second portion.